TECHNIQUES FOR PROVIDING MULTIPLE ON-CHIP TERMINATION IMPEDANCE VALUES TO PINS ON AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

[0092] Techniques are provided for matching the characteristic impedance of different transmission lines coupled to I/O pins on an integrated circuit. On-chip termination impedance circuitry can generate different termination impedance values for each I/O pin. Each termination impedance value is selected to match the characteristic impedance of the transmission line coupled to a particular I/O pin. The termination impedance can be set in response to the value of an off-chip resistor. Bit shifter circuitry can change the termination impedance provided to individual I/O pins. The bit shifter circuitry can increase or decrease the termination impedance at any of the I/O pins without changing the value of the off-chip resistor.